REMARKS

In response to the Office Action mailed December 7, 2005, Applicant respectfully requests reconsideration.

Claims 1-8 were previously pending in this application. By this amendment, Applicant amends claims 1, 2, 5, 6, and 8. As a result, claims 1-8 are pending for examination, of which claims 1, 5, 7 and 8 are independent. No new matter has been added.

Below, Applicants respond to contentions set forth in the Office Action only to the extent Applicants believe is necessary to place all of the claims in condition for allowance. Applicants' lack of response to any contention set forth in the Office Action should not be construed as Applicants' acquiescence to such contention.

1. Preliminary Remarks

Preliminarily, Applicants submit the following remarks with respect to the comments made in Section 2 of the Office Action (pages 2-4).

The Office Action asserts that Applicants "concluded that Hadjiyiannis does not disclose or suggest an assembler for a target microprocessor." Applicants made no such contention, but rather stated that "Hadjiyiannis does not disclose or suggest an assembler for a target microprocessor, **the assembler comprising, *inter alia*, a descriptor file containing information descriptive of the instruction set of said target microprocessor**." [bold emphasis added]. That is, Applicants never contended that Hadjiyiannis did not disclose or suggest an assembler, which Applicants readily concede it does. Rather, Applicants assert that Hadjiyiannis does not disclose or suggest an assembler comprising the full limitation of claim 1 set forth in quotes above.

The remainder of Section 2 of the Office Action obfuscates the well-known differences between source code (e.g., C and C+), intermediate code (e.g., SUIF), assembly code and machine code (i.e., binary code), and the different functions performed by the compiler and the assembler of Hadjiyiannis with respect to these types of code and ISDL. Applicants clarify these differences below only to the extent necessary to make clear the patentable distinctions between the claims and Hadjiyiannis, alone or in combination of Vos.

If, after this Amendment, the Examiner still maintains the rejections of claims 1-8, Applicants respectfully request that the Examiner contact Applicants' representatives to discuss these rejections further, including a more exhaustive treatment of the issues raised in Section 2 of the Office Action.

2. Claims 1-4 Patentably Distinguish over Hadjiyiannis

Claim 1 stands rejected under §102(b) as purportedly being anticipated by Hadjiyiannis et al, "ISDL: An Instruction Set Description Language for Re-targetability" (Hadjiyiannis). Applicants respectfully traverse this rejection.

Although Applicants believe that claim 1 patentably distinguished over Hadjiyiannis prior to this Amendment, by this Amendment, Applicants have amended claim 1 for further clarification and to expedite the prosecution of this application.

The discussion of Hadjiyiannis from Applicants' previous response mailed December 7, 2005, is hereby incorporated by reference. Hadjiyiannis discloses a language called ISDL (Instruction Set Description Language) that can be used to describe target architectures in a re-targetable compiler. The ISDL description of a target architecture can also be used to generate an assembler (Section III, paragraph 1, lines 7-8). Hadjiyiannis discloses that the authors have "designed and implemented an automatic assembler generator. It receives an ISDL description as input, and produces an assembler which assembles the compiler's output to a binary file."

Claim 1 as amended recites:

> An assembler for a target microprocessor, the assembler comprising:
> a descriptor file containing information descriptive of the instruction set of said target microprocessor;
> a translation device for translating assembly language into machine language as an output;
> a fetching device for acquiring data from said descriptor file; and
> **a control device arranged to receive said data from said fetching device and said machine language from said translation device, and operable to-constrain the machine language to conform to the architecture of said instruction set.** [emphasis added]

Claim 1 patentably distinguishes over Hadjiyiannis because Hadjiyiannis does not teach or suggest an assembler for a target microprocessor having all the limitations of the assembler recited

in claim 1, including the limitation of "a control device arranged to receive said data from said fetching device and said machine language from said translation device." The Office Action contends that such a control device is anticipated by the compiler of Hadjiyiannis (Office Action, page 6, lines 10-15). Applicants respectfully disagree. The compiler of Hadjiyiannis does not receive machine language as input. Rather, the compiler takes a high-level language as input. That is, "the compiler front-end receives a source program written in C or C++" (Section III, paragraph 1, lines 2-3). One of skill in the art that would readily understand that "a source program written in C or C++" is not machine language. Hadjiyiannis further discloses that "the compiler back-end takes the SUIF code as well as the ISDL description and produces assembly code." One of skill in the art would readily understand that SUIF (Stanford University Intermediate Format) code is a common intermediate format used to represent programs as part of the compilation process, and is not machine code. It is well known to those of skill in the art that machine code is produced by assembling assembly code, not vice versa. Therefore, as the compiler disclosed in Hadjiyiannis ultimately produces only assembly code, it is not possible that it receives machine code as input. For at least these reasons, the compiler of Hadjiyiannis is not "arranged to receive said data from said fetching device and said *machine language* from said translation device" as required by claim 1.

Hadjiyiannis also does not disclose or suggest a control device "operable to constrain the machine language to conform to the architecture of said instruction set," as recited in claim 1. Rather, the compiler of Hadjiyiannis "produces *assembly code* specific to, and optimized for, the target processor" (Section III, paragraph 1, lines 5-7). There is no mention that the compiler can operate on *machine language* to constrain the machine language to conform to the architecture of said instruction set. The terms "assembly code" and "machine language" are well known in the art, and a skilled person would appreciate that there is a very significant difference between operations performed on assembly code and those performed on machine language.

In view of the foregoing, claim 1 patentably distinguishes over Hadjiyiannis. Accordingly, Applicants respectfully request that the rejection of claim 1 under §102(b) as being anticipated by Hadjiyiannis be withdrawn. Claims 2-4 each depend from claim 1 and are patentable for at least the

same reasons. Accordingly, Applicants respectfully request that the rejections of these claims be withdrawn.

3. Claims 5-6 Patentably Distinguish Over Hadjiyiannis

Claim 5 stands rejected under §102(b) as purportedly being anticipated by Hadjiyiannis. Applicants respectfully traverse this rejection.

Claim 5 has been amended as shown above solely for clarification to recite:

> A method of assembling a machine language program for a target microprocessor comprising:
> providing a descriptor file containing information descriptive of the instruction set of said target microprocessor;
> translating assembly language instructions into machine language wherein the translation comprises;
> **directly transliterating the assembly language instructions to machine code**;
> acquiring data from said descriptor file; and
> **constraining the directly transliterated machine language to conform to the architecture of said instruction set**, thereby assembling the machine language program for the target microprocessor.
> [emphasis added]

Hadjiyiannis does not teach or suggest a method of assembling a machine language program for a target microprocessor comprising, *inter alia,* directly transliterating the assembly language instructions to machine language, and constraining the directly transliterated machine language to conform to the architecture of said instruction set, as recited in claim 5. Hadjiyiannis makes abundantly clear throughout that generating assembly code from source code is a separate, discrete operation from generating binary code (i.e., machine code) from assembly code. Specifically, Hadjiyiannis discloses a compiler that generates assembly code from source code (e.g., C or C++) and an (automatically generated) assembler that generates binary code from the assembly code. (Section III, paragraph 1). The compiler uses the ISDL description to generate the assembly code, and to generate the assembler itself. However, the assembler does not use the ISDL description when generating the binary file from the assembly code. That is, Hadjiyiannis does not teach or suggest using the ISDL description in any way during the translation from assembly language to

machine language, much less in constraining directly transliterated machine language to conform to the ISDL description.

In view of the foregoing, claim 5 patentably distinguishes over Hadjiyiannis. Accordingly, Applicants respectfully request that the rejection of claim 5 under §102(b) as being anticipated by Hadjiyiannis be withdrawn. Claim 6 depends from claim 5 and is patentable over Hadjiyiannis for at least the same reasons. Accordingly, Applicants respectfully request that the rejection of claim 6 under §102(b) be withdrawn.

4. Claim 7 Patentably Distinguishes Over Hadjiyiannis in View of Vos

Claim 7 stands rejected under §103(a) as purportedly being unpatentable over Hadjiyiannis in further view of U.K. Patent No. GB 2,127,188 (Vos). Applicants respectfully traverse this rejection.

The combination of Hadjiyiannis and Vos is improper because, at the time of the invention, one of skill in the art would not have been motivated to combine Hadjiyiannis and Vos as suggested in the Office Action. Further, even if such combination were proper (which it is not), claim 7 would patentably distinguish over such combination.

Claim 7 recites:

> A method of preparing a program executable on a target microprocessor comprising:
>
> **capturing data from the instruction set of said target microprocessor thereby forming a descriptor file containing information descriptive of said instruction set;**
>
> providing assembly language instructions for said target microprocessor;
>
> translating each assembly language instruction into a corresponding machine language output; and
>
> **using data from said descriptor file, constraining the machine language output to conform to the architecture of said instruction set.**

As set forth in Applicants previous response, the combination of Hadjiyiannis and Vos do not teach or suggest the step of "capturing data from the instruction set of said target microprocessor thereby forming a descriptor file containing information descriptive of said instruction set." As set forth in the previous response, Vos fails to remedy the deficiencies of Hadjiyiannis in disclosing this

limitation in claim 7, as Vos is silent regarding the use of an instruction set of a target microprocessor to form a descriptor file containing information descriptive of said instruction set.

Further, the asserted combination of references doe not teach or suggest a method of preparing a program executable on a target microprocessor comprising, *inter alia*, "using data from said descriptor file, constraining the *machine language* output to conform to the architecture of said instruction set." Rather, as is made clear above, the ISDL description is not used in any fashion to constrain the binary file generated by the assembler. Vos fails to remedy this deficiency of Hadjiyiannis.

In view of the foregoing, claim 7 patentably distinguishes over the combination of Hadjiyiannis and Vos. Accordingly, Applicants respectfully request that the rejection of claim 7 under §103(a) be withdrawn.

5. Claim 8 Patentably Distinguishes over Hadjiyiannis in View of Vos

Claim 8 stands rejected under §103(a) as purportedly being unpatentable over Hadjiyiannis in further view of Vos. Applicants respectfully traverse this rejection.

The combination of Hadjiyiannis and Vos is improper for the reasons set forth above. Further, even if the combination were proper (which it is not), claim 8 would distinguish over such combination.

Claim 8 has been amended as shown above solely for clarification. Claim 8 patentably distinguishes over Hadjiyiannis in view of Vos for reasons that should be clear from the discussion of Hadjiyiannis and Vos set forth above in Section III. Specifically, the combination of Hadjiyiannis and Vos does not teach or suggest a method of preparing a program executable on a microprocessor, comprising, *inter alia*, translating assembly language instructions into machine language wherein the translation step comprises **directly transliterating the assembly language instructions to machine language**; acquiring data from said descriptor file; and **constraining the directly transliterated machine language to conform to the architecture of said instruction set**, as required by claim 8.

In view of the foregoing, claim 8 patentably distinguishes over Hadjiyiannis in view of Vos. Accordingly, Applicants respectfully request that the rejection of claim 8 under §103(a) be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: March 7, 2006

Respectfully submitted,

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